IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sudhakar Kale et al.   Examiner: Unknown
Serial No.: Unknown   Group Art Unit: Unknown
Filed: Herewith   Docket: 884.142US2
Title: STRUCTURAL REGULARITY EXTRACTION AND FLOORPLANNING IN
             DATAPATH CIRCUITS USING VECTORS

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 09/435,112, filed on November 5, 1999, which is relied upon for an earlier filing date under 35 U.S.C. §120.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

SUDHAKAR KALE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9592

Date _July 14, 2003_   By _Ann M. McCrackin_
                                                   Ann M. McCrackin
                                                   Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Patent Application, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14th day of July, 2003

Kacia Lee   _Kacia Lee_

Name   Signature

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(Use as many sheets as necessary)

Complete if Known	
Application Number	Unknown
Filing Date	Even Date Herewith
First Named Inventor	Kale, Sudhakar
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 2

Attorney Docket No: 884.142US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-5,652,874	07/29/1997	Upson, et al.	395	500	06/07/1995
	US-5,737,237	04/07/1998	Tanaka, et al.	364	491	02/16/1996
	US-5,838,583	11/17/1998	Varadarajan, Ravi, et al.	364	491	04/12/1996
	US-5,898,595	04/27/1999	Bair, et al.	364	491	05/26/1995
	US-5,910,898	06/08/1999	Johannsen,	364	489	12/14/1995
	US-5,926,398	07/20/1999	Nakamura, Takeshi	364	491	03/03/1997
	US-5,930,499	07/27/1999	Chen, Yulin, et al.	395	500.09	05/20/1996
	US-5,991,524	11/23/1999	Belkhale, et al.	395	500.19	04/14/1997
	US-6,066,178	05/23/2000	Bair, O. S., et al.	716	2	04/10/1996
	US-6,148,433	11/14/2000	Chowdhary, A., et al.	716	1	11/06/1998
	US-6,189,131	02/13/2001	Graef, S., et al.	716	8	01/14/1998
	US-6,230,303	05/08/2001	Dave, B. P.	716	7	02/17/1998
	US-6,237,129	05/01/2001	Patterson, et al.	716	8	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T^2

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T^2
		ARIKATI, SRINIVASA R., et al., "A Signature Based Approach to Regularity Extraction", Proceedings IEEE International Conference on CAD, (Nov. 1997),542-545	
		CHOWDHARY, AMIT, et al., "A General Approach for Regularity Extraction in Datapath Circuits", ICCAD, (Nov. 1998),	
		CHOWDHARY, AMIT, et al., "Extraction of Functional Regularity in Datapath Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, (Sept. 1999),1279-1296	
		CHOWDHARY, AMIT, et al., "Extraction of Functional Regularity in Datapath Circuits", IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 18, NO. 9, SEPTEMBER 1999, XP-002191876,1279-1296	
		CHOWDHARY, AMIT, et al., "Technology Mapping for Field-Programmable Gate Arrays Using Integer Programming", Proceedings IEEE International Conference on CAD, (Nov. 1995),346-352	
		CORAZAO, MIGUEL R., et al., "Performance Optimization Using Template Mapping for Datapath-Intensive High-Level Synthesis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, 8, (Aug.	

EXAMINER		DATE CONSIDERED	

Substitute for form 1449A/PTO **INFORMATION DISCLOSURE** **STATEMENT BY APPLICANT** *(Use as many sheets as necessary)*	*Complete if Known*	
	Application Numb r	Unknown
	Filing Date	Even Date Herewith
	First Named Inventor	Kale, Sudhakar
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 2 of 2	**Attorney Docket No: 884.142US2**	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		1996),877-888	
		DETJENS, EWALD, et al., "Technology Mapping in MIS", Proceedings IEEE International Conference on CAD, (1987),116-119	
		DOBBERPUHL, DANIEL W., "Circuits and Technology for Digital's StrongARM and ALPHA Microprocessors", Proceedings Seventeenth Conference on Advanced Research in VLSI, (Sept. 15-16 1997),2-11	
		GUPTA, RAJESH K., et al., "Using a Programming Language for Digital System Design", IEEE Design & Test of Computers, (April 1997),72-80	
		HANSEN, MARK C., et al., "High-Level Test Generation using Physically-Induced Faults", 13th IEEE VLSI Test Symposium, (May 1995),20-28	
		HIRSCH, MARK, et al., "Automatically Extracting Structure from a Logical Design", Proceedings IEEE International Conference on CAD, (Nov. 1988),456-459	
		KEUTZER, KURT, "DAGON: Technology Binding and Local Optimization by DAG Matching", Proceedings 24th Design Automation Conference, (June 1987),341-347	
		LI, JIAN, et al., "HDL Code Restructuring Using Timed Decision Tables", Proceedings of the Sixth International Workshop on Hardware/Software Codesign, (March 1998),131-135	
		NIJSSEN, R.X.T., et al., "GreyHound: A Methodology for Utilizing Datapath Regularity in Standard Design Flows", INTEGRATION, the VLSI Journal 25, (1998),111-135	
		NIJSSEN, R.X.T., et al., "Regular Layout Generation of Logically Optimized Datapaths", Proceedings International Symposium on Physical Design, (1997),42-47	
		ODAWARA, GOTARO, et al., "Partitioning and Placement Technique for CMOS Gate Arrays", IEEE Transactions on Computer-Aided Design, Vol. CAD-6, 3, (May 1987),355-363	
		RABAEY, J. M., et al., "Fast Prototyping of Datapath-Intensive Architectures", IEEE Design & Test of Computers, (June 1991),40-51	
		RAO, D. SREENIVASA, et al., "An Approach to Scheduling and Allocation Using Regularity Extraction", IEEE, (1993),557-531	
		RAO, D. S., et al., "On Clustering for Maximal Regularity Extraction", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, 8, (Aug. 1993),1198-1208	
		YALCIN, HAKAN, et al., "An Approximate Timing Analysis Method for Datapath Circuits", Proceedings IEEE International Conference on CAD, (Nov. 1996),114-118	

EXAMINER	**DATE CONSIDERED**